IN THE CLAIMS

1. (Original) A circuit comprising:

a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay;

a forward path connected to the measuring path for delaying the reference signal based on the measured delay to generate an internal signal; and

a feedback path connected to the measuring path and the forward path, the feedback path including a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal, wherein the calibrating unit is configured to conditionally adjust a pulse width of the pulse.

2. (Original) The circuit of claim 1, wherein the calibrating unit includes a selectable delay segment for delaying the reference signal to generate a first feedback signal of the plurality of feedback signals.

3. (Original) The circuit of claim 2, wherein the calibrating unit further includes a model delay segment for generating a second feedback signal of the plurality of feedback signals.

4. (Original) The circuit of claim 3, wherein the selectable delay segment includes a chain of delay elements.

5. (Original) The circuit of claim 4, wherein the model delay segment includes a chain of delay elements.

6. (Original) The circuit of claim 3, wherein the calibrating unit further includes a generator connected to the selectable delay segment and the model delay segment for generating the pulse based on the first and second feedback signals.

7. (Original) The circuit of claim 1, wherein the measuring path includes a monitoring unit for enabling the calibrating unit to adjust the pulse width of the pulse.

8. (Original) The circuit of claim 7, wherein the measuring path further includes a measuring unit for propagating the pulse.

9. (Original) The circuit of claim 8, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is adjusted.

10-20. (Canceled)

21. (Original) A memory device comprising:

a memory array for storing data;

an output data path for outputting the data; and

a delay lock circuit connected to the data path for providing an internal signal to control a transfer of data at the output data path, the delay lock circuit including:

a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay;

a forward path connected to the measuring path for delaying the reference signal based on the measured delay to generate the internal signal; and

a feedback path connected to the measuring path and the forward path, the feedback path including a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal, wherein the calibrating unit is configured to conditionally adjust a pulse width of the pulse.

22. (Original) The memory device of claim 21, wherein the calibrating unit includes a selectable delay segment for delaying the reference signal to generate a first feedback signal of the plurality of feedback signals.

23. (Original) The memory device of claim 22, wherein the calibrating unit further includes a model delay segment for generating a second feedback signal of the plurality of feedback signals.

24. (Original) The memory device of claim 23, wherein the calibrating unit further includes a generator connected to the selectable delay segment and the model delay segment for generating the pulse based on the first and second feedback signals.

25. (Original) The memory device of claim 24, wherein the selectable delay segment includes a chain of delay elements.

26. (Original) The memory device of claim 25, wherein the model delay segment includes a chain of delay elements.

27. (Original) The memory device of claim 21, wherein the measuring path includes a monitoring unit for enabling the calibrating unit to adjust the pulse width of the pulse.

28. (Original) The memory device of claim 27, wherein the measuring path further includes a measuring unit for propagating the pulse.

29. (Original) The memory device of claim 28, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is adjusted.

30-44. (Canceled)

45. (Original) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a memory array for storing data;

an output data path for outputting the data; and

a delay lock circuit connected to the data path for providing an internal signal to control a transfer of data at the output data path, the delay lock circuit including:

a measuring path for receiving a reference signal to sample a pulse to obtain a measured delay;

a forward path connected to the measuring path for delaying the reference signal based on the measured delay to generate the internal signal; and

a feedback path connected to the measuring path and the forward path, the feedback path including a calibrating unit for generating the pulse based on a plurality of feedback signals generated from the reference signal, wherein the calibrating unit is configured to conditionally adjust a pulse width of the pulse.

46. (Original) The system of claim 45, wherein the calibrating unit includes a selectable delay segment for delaying the reference signal to generate a first feedback signal of the plurality of feedback signals.

47. (Original) The system of claim 46, wherein the calibrating unit further includes a model delay segment for generating a second feedback signal of the plurality of feedback signals.

48. (Original) The system of claim 47, wherein each of the selectable delay segment and the model delay segment includes a chain of delay elements.

49. (Original) The system of claim 47, wherein the calibrating unit further includes a generator connected to the selectable delay segment and the model delay segment for generating the pulse based on the first and second feedback signals.

50. (Original) The system of claim 45, wherein the measuring path includes a monitoring unit for enabling the calibrating unit to adjust the pulse width of the pulse.

51. (Original) The system of claim 50, wherein the measuring path further includes a measuring unit for propagating the pulse.

52. (Original) The system of claim 51, wherein the monitoring unit is configured to reset the measuring unit when the pulse width is adjusted.

53-59. (Canceled)